

# Gain-adjustment Technique for Resonant Power Converters with Piezoelectric Transformer

Joung-hu Park, Sungjin Choi, Sangmin Lee and Bo H. Cho

School of Electrical Engineering and Computer Science  
Seoul National University Eng. 420-043, San 56-1, Shillim-dong  
Kwanak-Ku, Seoul 151-744, Korea

**Abstract**— In power processing applications, switching power converter research have focused on the potential feasibility of piezoelectric transformers (PTs) for cost competitiveness, size effect and good EMI characteristics. However, the PT has a voltage conversion limit because of its physical dimensions and manufacturing procedures. The fact can be a restriction to a circuit engineer facing new application design with PT because of its inadaptivity to extreme conversion ratios of emerging applications.

In order to overcome this problem, tapped inductor is introduced. The tapped inductor can transform the input voltage into the adequate level by its own turn-ratio. Consequently, this tapped inductor scheme with piezoelectric transformer makes it possible to obtain both PT's advantages and conversion gain adjustment without part-count increase. For the proposed converter evaluation, this paper provides the operation analysis and design procedures of the converter, and presents the experimental verification with a 20-W hardware prototype DC/DC converter as well. Finally, topology extension is also presented by combining tapped-inductor with other conventional resonant converters with piezoelectric transformer.

**Index Terms**— Piezoelectric Transformer, Tapped-inductor, Resonant Converter, Gain-adjustment

## I. INTRODUCTION

Nowadays, the Piezoelectric Transformer (PT) is widely used in power applications. The market portion increases as a good alternative solution to magnetic transformer due to its low profile and no winding characteristics. However, since the voltage gain of a PT is determined mainly by the size of the electrodes, the number of secondary layers as well as by the dielectric, mechanical, and piezoelectric constants of the material [1], the gain that a PT can handle has a limitation. As another solution, PT can be highly multi-layered for handling an extreme gain [2]. However, the manufacturing cost increases exponentially according to the number of the layers. In order to obtain both extreme voltage conversion-ratio and cost-competitiveness, especially for resonant switching converters, this paper suggests a tapped-inductor application replacing previous untapped AC inductor.

For the resonant converter, a 20W radial-mode disk-type PT (Fig. 1(a)) is used as a main step-down power-processing transformer in this paper. The primary electrode placed in the center, and the secondary

electrode are concentrically arranged in the outer part of the disk and spaced from the input electrode. The disk is polarized in the axial direction and thus, is perpendicular to the plane of electrodes. This device can be operated in the fundamental radial or the first overtone resonance. The fundamental resonant frequency is around 60kHz and the secondary resonant frequency is about 150kHz [1]. Figure 1(b) shows the equivalent circuit model of the PT and the detail analysis is performed using these model parameters. The parameters  $L_m$ ,  $C_m$ ,  $R_m$  are equivalent to the mechanical resonance of the PT, and  $C_i$  and  $C_o$  are the capacitances of the primary and secondary electrodes, respectively [3]. The purpose of this paper is the operation analysis of the tapped-inductor resonant converter with piezoelectric transformer, especially about the gain-adjustment issues. The analysis is verified by the hardware experiments with 20W DC/DC prototype converter.

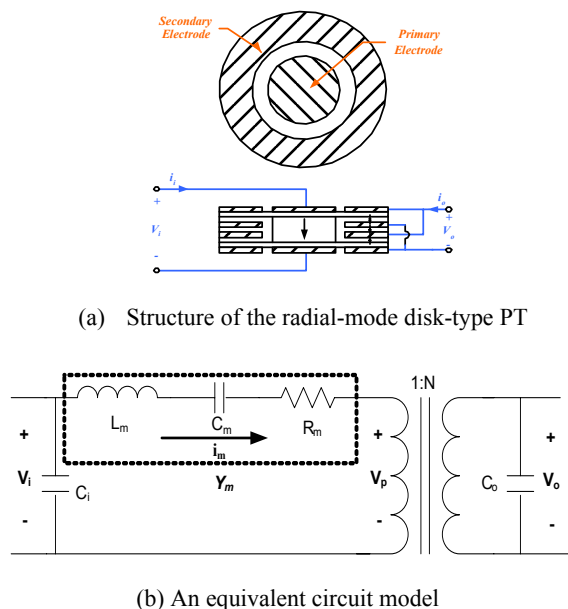
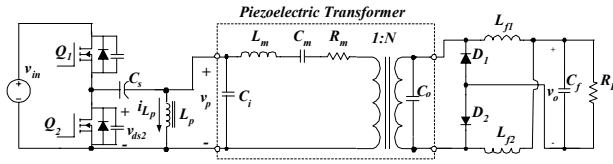
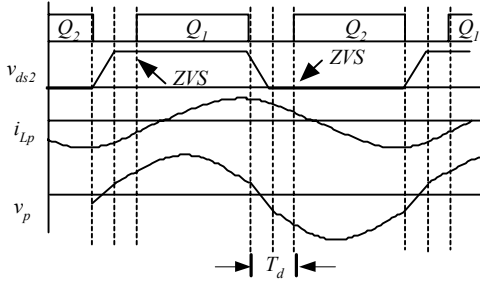


Fig. 1 Physical configuration and equivalent circuit model for the Piezoelectric Transformer [4]



(a) Circuit diagram with PT equivalent model



(b) Key waveforms of the resonant converter

Fig. 2. The conventional pseudo-resonant (Cs-Lp type) half-bridge dc/dc converter using PT [5]

#### A. Conventional PT converter[5]

For a good example of PT resonant converter, the conventional pseudo-resonant (Cs-Lp type) half-bridge converter is shown in Fig. 2. In this circuit, the resonant network is composed of capacitance  $C_s$ , together with the parallel inductance  $L_p$ , and provides a nearly sinusoidal waveform to the PT. The converter regulates output voltage only by frequency control, and the duty cycles of the high side and the low side switches are symmetrical with 180-degree phase-shift and dead-time  $T_d$  as other typical half-bridge circuits have. Figure 2(b) shows the key-waveforms described above. In the figure, it is shown that soft-switching operation (ZVS) is achieved in both Q1 and Q2 switches for high efficiency. This circuit was proposed for small inductor  $L_p$  due to the decrease of circulating energy through the inductor, compared to  $L_s$  type that has resonant inductor connected to PT in series.

#### B. Proposed PT resonant converter

In this paper, in order to enhance the voltage conversion ratio of the conventional converter into an irregular PT gain range without additional components or harsh PT design, tapped-inductor is introduced as one of the effective solutions for cost-size optimization. Many previous researches have proposed tapped-inductor application for conventional switching converters with extreme conversion ratios [6-9]. The structure of the tapped-inductor is a simple variation of the basic coupled-inductor that the primary and secondary share a copper winding by tapping in the middle of single winding (Fig. 3), different from the separate winding of isolated transformer. Since the tapped inductor operates like an autotransformer without reset circuit as well as

like an inductor storing up the circulating energy, it is available to change input-output conversion ratios without extra part-count. Even though tapped-inductor excludes electrical isolation property, PT compensates the problem with the inherent transformer inside the body.

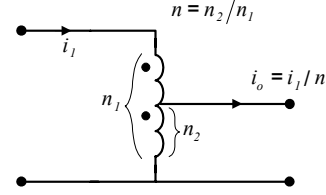


Fig. 3 Tapped-inductor configuration

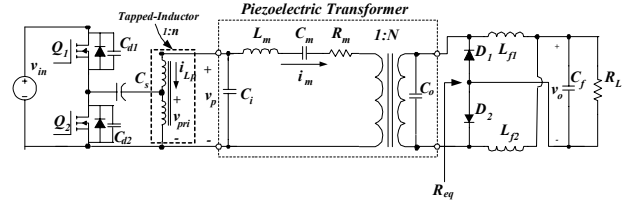


Fig. 4 Proposed Cs-Lp type DC/DC converter using a tapped-inductor

The proposed converter employing tapped inductor ( $n > 1$ ) is shown in Fig. 4. The key waveform is the same as those in Fig. 2(b). During the switch on/off stage, the series capacitance,  $C_s$ , resonates with the parallel inductance,  $L_p$  (secondary), which provides a nearly sinusoidal voltage to the PT primary side. Because the PT has a very high resonant quality factor, it is assumed that the input current  $i_m(t)$  is pure sinusoidal and denoted to  $I_m$  at time  $t=0$ , then

$$i_m(t) = I_m \cos(\omega t) \quad (1)$$

where,  $\omega$  is the switching frequency of the circuit[4].

When the high-side switch is turned on at  $t=t_1$ , the primary voltage of the PT and the parallel inductor current are given by:

$$v_p(t) = K_2 I_m \cdot \frac{1}{\omega \cdot (C_s / n^2 + C_i)} \cdot \sin[\omega(t-t_1)] + Z_o [K_1 I_m - I_{Lp0}] \cdot \sin[\omega_o(t-t_1)] + V_{p0} \cdot \cos[\omega_o(t-t_1)] \quad (2)$$

$$i_{Lp}(t) = -K_2 I_m \left( \frac{\omega_o}{\omega} \right)^2 \cdot \cos[\omega(t-t_1)] - (K_1 I_m - I_{Lp0}) \cdot \cos[\omega_o(t-t_1)] + \left( \frac{V_{p0}}{Z_o} \right) \sin[\omega_o(t-t_1)]$$

$$K_1 = \frac{1}{\left( \frac{\omega}{\omega_o} \right)^2 - 1}, K_2 = \frac{1}{\left( \frac{\omega_o}{\omega} \right)^2 - 1}, \omega_o = \frac{1}{\sqrt{L_p (C_s / n^2 + C_i)}}, Z_o = \sqrt{\frac{L_p}{C_s / n^2 + C_i}}$$

where,  $V_{p0}$  and  $I_{Lp0}$  are initial values of the resonant period. If  $\omega_o \approx \omega$ ,  $i_{Lp}$  can be simplified:

$$i_{Lp}(t) = I_{Lp0} \cos[\omega_o(t-t_1)] + \left( \frac{V_{p0}}{Z_o} \right) \sin[\omega_o(t-t_1)] \quad (3)$$

The low-side turns on has similar waveform as (2), thus piecewise sinusoidal steady-state waveforms with low harmonic components are generated by this topology. In the following section, the design guideline of the proposed converter will be presented using these equations.

### III. DESIGN GUIDELINE

The design guideline is exactly the same as the conventional one except the inductor design. Hence, only the inductor design is presented with selection of turn-ratio and inductance. The comparison with conventional inductor design is also included.

#### A. Turn ratio $n$

The turn ratio can be determined from the converter voltage conversion ratios. The ratios are derived from the two steps such as PT-input stage gain and output stage gain. As for the output stage gain, the gain is derived from the equivalent circuit (fig. 1(b)) as:

$$\frac{V_o}{V_{pri}} = n \cdot \frac{sC_m R_{eq}}{N^2(1 + sC_o R_{eq})(s^2 L_m C_m + sC_m R_m + 1) + sC_m R_{eq}} \quad (4)$$

When  $C_s$  is relatively large, the primary winding resonant voltage magnitude,  $V_{pri}$ , can be approximated by the fundamental harmonic of  $v_{pri}$  in Fig. 4 as follows:

$$V_{pri} \approx V_{in} \cdot \left(\frac{2}{\pi}\right) \cdot \frac{\sin(\pi \frac{T_d}{T})}{\pi \frac{T_d}{T}} \quad (5)$$

From (4) and (5), the overall converter gain can be calculated, which is controlled by the tapped-inductor turn ratio  $n$ .

$$\frac{V_o}{V_{in}} = n \cdot \frac{sC_m R_{eq}}{N^2(1 + sC_o R_{eq})(s^2 L_m C_m + sC_m R_m + 1) + sC_m R_{eq}} \cdot \left(\frac{2}{\pi}\right) \cdot \frac{\sin(\pi \frac{T_d}{T})}{\pi \frac{T_d}{T}} \quad (6)$$

#### B. Inductance $L_p$

The tapped-inductor secondary inductance  $L_p$  is designed by soft-switching condition. To obtain ZVS operation in the MOSFETs  $Q_1$ ,  $Q_2$ , their parasitic capacitances  $C_{d1}$ ,  $C_{d2}$  should be fully charged or discharged during  $T_d$  [1]. The charging and discharging current flow through the parallel inductor,  $L_p$ . Since the time interval is relatively short to entire switching cycle, the current can be considered constant and the switch drain-source voltage is a near quasi-square waveform. From those assumptions, minimum inductor current ( $I_{req}$ ) for soft-switching is given by;

$$I_{req} = C_{eq} \frac{v_{in}}{T_d} \quad C_{eq} \approx C_{ds1} + C_{ds2} + n^2 C_i \quad (7)$$

where  $v_{in}$  is the input voltage.

The actual inductor current ( $I_{L0}$ ) at the beginning of the dead-time region can be approximated with the assumption that the switching frequency of the converter is near the resonant frequency of the PT, such as:

$$I_{L0} = \frac{V_{pri}}{\omega \cdot (L_p / n^2)} \cdot \cos(\pi \frac{T_d}{T}) = \left(\frac{2}{\pi}\right) \cdot \frac{\sin(2\pi \frac{T_d}{T})}{2\pi \frac{T_d}{T}} \cdot \frac{V_{in}}{\omega \cdot (L_p / n^2)} \quad (8)$$

For the soft-switching operation, the actual current should be greater than the required one. From (7) and (8), the inductance design equation for ZVS is derived. The maximum  $L_p$  should be designed as:

$$L_p \leq \left(\frac{2}{\pi}\right) \cdot \frac{\sin(2\pi \frac{T_d}{T})}{2\pi \frac{T_d}{T}} \cdot \frac{T_d \cdot T}{2\pi \cdot C_{eq}} \cdot n^2 \quad (9)$$

#### C. Comparison to the conventional design

For the size and cost estimation, the inductor design is compared between conventional untapped and tapped. The inductor size is dominantly determined by core selection with the assumption that winding area is enough for the copper winding. For core selection,  $K_C$ , the core geometrical constant is presented as [10]:

$$K_C \geq \frac{\rho L_p^2 I_{max}^2}{B_{max}^2 R K_u} \cdot 10^8 \quad (cm^5) \quad (10)$$

where,  $\rho$ : Wire resistivity,  $I_{max}$ : peak winding current,  $L_p$ : primary inductance,  $R$ : winding resistance,  $K_u$ : winding fill factor,  $B_{max}$ : Maximum operating flux density. Considering the minimum  $K_C$ , the inductance and current that changes according to the turn ratio design have an effect on the constant value. However, when the resonant frequency  $1/(L_p C_{eq})^{1/2}$  is restrained constant whatever  $n$  is, the geometrical constant is almost the same because  $I_{Lp}$  is dominantly affected by resonant impedance  $Z_o$  (see (3)). Therefore, the inductor size are similar each other if it is tapped or not, and the optimal converter design is possible by relieving harsh PT implementation as well.

### IV. EXPERIMENTAL RESULTS

A 20W converter hardware of proposed  $C_s$ -  $L_p$  type series-resonant half-bridge with tapped-inductor was used for experimental verification of the operation analysis and design guideline. Current doubler is used as the output rectifier shown in Fig. 4. The equivalent load  $R_{eq}$  ( $= \pi^2 R_L / 2$ ) was fixed at the optimal load of the PT (49.3 $\Omega$ ). The major circuit components and PT parameter values are shown in Table I. The inductor core is PQ2020 at every turn-ratios ( $n=0.5, 1, 2$ ). Figure 5 shows the hardware prototype. The converter is composed of pre-stage AC/DC converter and isolated DC/DC converter. In fact, the 24cm-length layout PCB was design for 40W off-line converter with multi-connected two 20W PTs. However, since the multi-connected output of PTs causes gain variation by phase deviation between the PTs, only single PT was used to eliminate the effect.

Figure 6 shows the experimental results. Figure 6(a) shows the PT-driving waveforms. The drain-to-source voltage ( $V_{ds2}$ ) is a trapezoidal shape that accomplishes a ZVS operation successfully, and the tapped-inductor input waveform ( $V_{pri}$ ) dominantly includes the switching-

frequency fundamental component. Figure 6(b) shows the voltage gain curves according to the operating frequency and tapped-inductor turn-ratios. With the twice turn-ratio ( $n=2$ ), the maximum voltage gain (13.06) is also almost twice (6.69) of the unity case ( $n=1$ ). If  $n=0.5$ , the gain becomes half the level (3.03). From controlling  $n$ , the voltage gain can be adjusted into any required range even with the same PT. In summary, the tapped-inductor gives an additional design freedom for the PT-employed power converter and guarantees more optimal design so that the system requirements can be satisfied even in extreme input-voltage ranges.

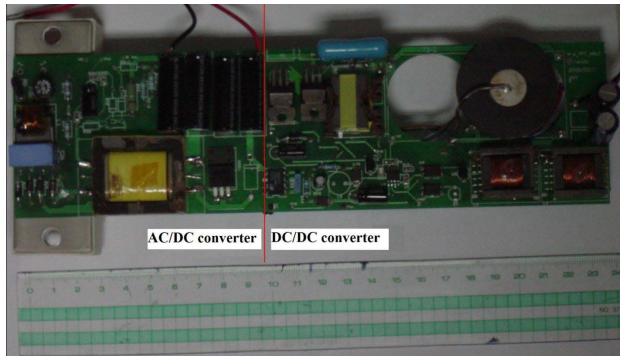
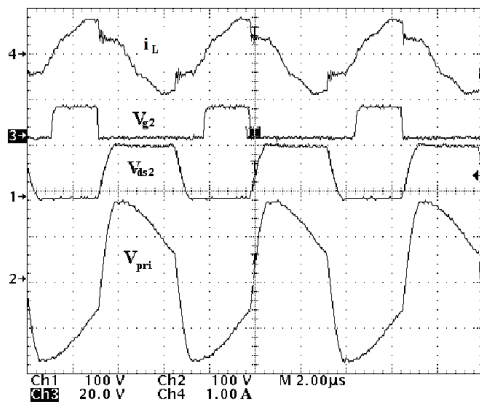
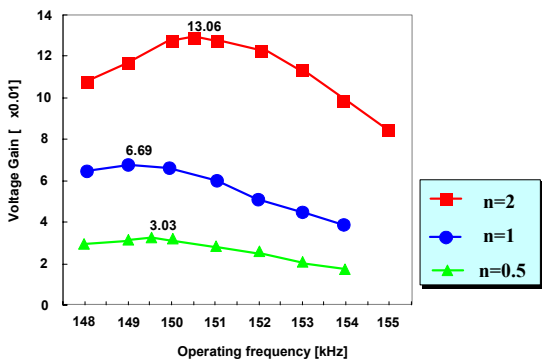


Fig. 5. Hardware Prototype



(a) Key waveforms of the hardware prototype



(b) Voltage gain vs. operating frequency

Fig. 6 Hardware experiment results

## V. EXTENDED APPLICATIONS

This tapped-inductor can be applied to other conventional resonant PT converter circuits [11-13]. If a converter includes resonant inductor connected series or parallel with PT, tapped-inductor can replace the conventional inductor without the operating mode change. Figures 7-9 show the tapped-inductor employed PT resonant converters. These converters conserve the previous operation principles and part count except the voltage conversion ratio.

Figure 10 shows an input-parallel output-series PT-connected converter with tapped-inductor in primary side. Since input-parallel output-series scheme has better thermal characteristics than parallel-parallel connection, it has been researched as a good alternative for power capacity enhancement [14]. However, the entire converter voltage gain becomes twice as great as that of the single PT at the optimal efficiency operation. In that case, the gain can be adjusted into the half by tapped inductor ( $n=0.5$ ) which makes the output voltage also half of each PT. Then, the optimal load condition can also be obtained by an extra capacitor connected parallel to the output side of each PT. This method shows the possibility that optimal design of the arbitrary severe gain and load conditions can be guaranteed with conventional mass-product PT devices.

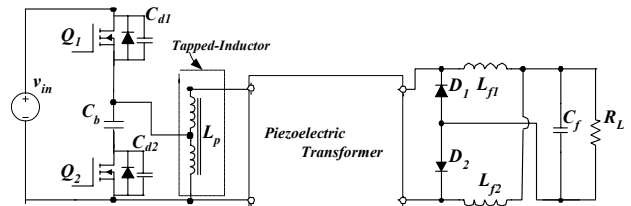


Fig. 7. Clamp-type constant-frequency PWM half-bridge converter with tapped-inductor

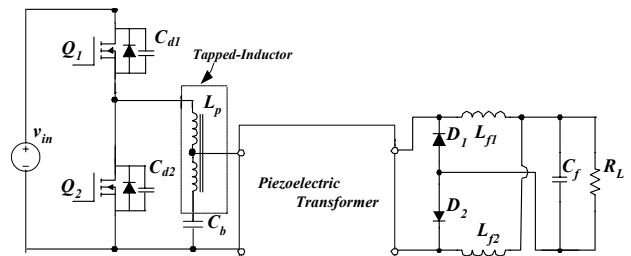


Fig. 8. Square-wave ZVS converter with tapped-inductor

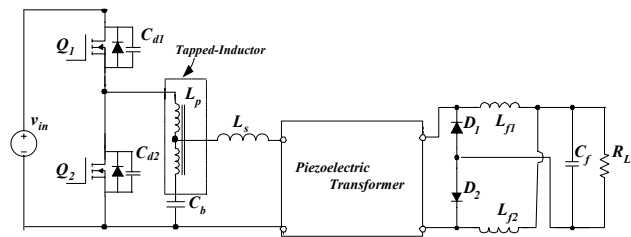


Fig. 9. A variation of resonant PT converter in Fig. 8 with reduced circulating energy

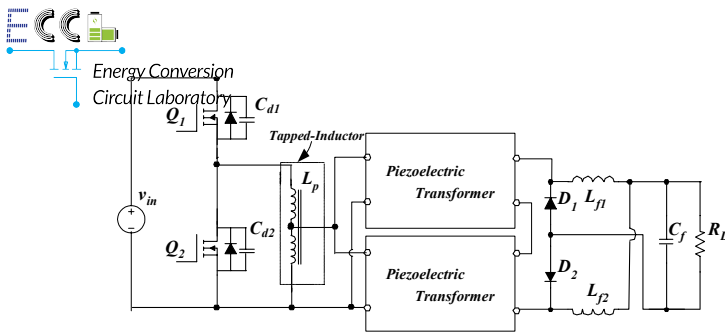


Fig. 10. Multi-connected PT converter (Parallel-series connection)

TABLE I. Major parameter values

Parameter	Value
$L_m$	16.7mH
$C_m$	70.8pF
$R_m$	51.5 $\Omega$
$C_i$	755pF
$C_o$	18.5nF
$N$	0.20
$n$	1, 0.5, 2
$L_p$	170uH, 60uH, 240uH

## VI. CONCLUSIONS

In this paper, a gain-adjustment technique using tapped inductor is proposed for resonant converter with piezoelectric transformer. Without part-count and volume increase, the proposed technique provides the improvement of voltage conversion range which is restricted by the gain limitation of piezoelectric transformer design. The proposed topology in which tapped inductor is employed to the conventional resonant converter, is more adaptable for the universal-input power application because one more design freedom coming from the turn ratio variable provides wider gain ranges than that conventional one has. Its operation and performance analysis were verified by a 20W hardware prototype. Also, this technique is applied to other resonant converter topologies for extended gain adjustment.

## REFERENCES

- [1] Sungjin Choi, *Modeling and Analysis of Disk-type Piezoelectric Transformer and its Application of Off-line Power Converters*, Ph.D. dissertation, Seoul National University, Seoul, Korea, Feb. 2006.
- [2] Hoonbum Shin, Hyungkeun Ahn, Deuk-Young Han, "Design Analysis of Step-down Multilayer Piezoelectric Transformer," *JOURNAL OF POWER ELECTRONICS*, Vol. 3, No. 3, pp. 139 ~ 144, 2003. 7
- [3] T. Zaitzu, T. Inoue, O. Ohnishi, A. Iwamoto, "2 MHz power converter with piezoelectric ceramic transformer," *INTELEC '92*, pp. 430 - 437, Oct. 1992.
- [4] S. J. Choi, T. I. Kim, S. M. Lee and Bo H. Cho, "Modeling and Characterization of Radial-mode Disk-type Piezoelectric Transformer for AC/DC Adapter," *PESC05*, pp. 624-629, Jun 2005.

- [5] S. J. Choi, T. I. Kim, B.H. Cho, "Design of Half-Bridge Piezo-Transformer Converters in the AC Adapter Applications" *APEC05*, Vol 1, pp. 244-248, Mar 2005.
- [6] Jia Wei, Peng Xu, Ho-Pu Wu, Fred C. Lee, Kaiwei Yao, Mao Ye, "Comparison of Three Topology Candidates for 12V VRM," *IEEE APEC*, Page(s): 245 - 251, 2001.
- [7] M. Rico, J. Uceda, J. Sebastian, and F. Aldana, "Static and Dynamic Modeling of Tapped-Inductor DC-to-DC Converters," *IEEE PESC*, Page(s): 281-287, 1987.
- [8] Edry, D., Hadar, M., Mor, O., Ben-Yaakov, S., "A SPICE compatible model of tapped-inductor PWM converters," *Applied Power Electronics Conference*, vol.2, Page(s): 1021 - 1027, 1994.
- [9] Jong-Hu Park and B. -H. Cho, "The zero Voltage-switching (ZVS) critical conduction mode(CRM) buck Converter with tapped-inductor", *Power Electronics, IEEE Transaction on*, Vol.20, Issue 4, pp. 762-774, July 2005.
- [10] Robert W. Erickson, Daragan Maksimovic, *Fundamentals of power electronics*, Kluwer Academic Publishers, 1999.
- [11] Myounghwan Ryu; Sungjin Choi; Sangmin Lee; Cho, B.H., "A new piezoelectric transformer driving topology for universal input AC/DC adapter using a constant frequency PWM control," *Applied Power Electronics Conference and Exposition, Twenty-First Annual IEEE*, Page(s): 1314-1317, 19-23 March 2006.
- [12] T. Zaitzu, O. Ohnishi, T. Inoue, M. Shoyama, .Ninomiya, F.C.Lee, and G.C.Hua, "Piezoelectric Transformer operating in Thickness Extensional Vibration and its Application to Switching Converter," *PESC '94 Record, 25th Annual IEEE*, vol.1, Page(s):585 - 589, 20-25 June 1994.
- [13] Tmotsu Ninomiya, Masahito Shoyama, Toshiyuki Zaitzu, and Takeshi Inoue, "Zero-Voltage-Switching Techniques and their Application to High-Frequency Converter with Piezoelectric Transformer," *IECON '94, 20th International Conference on*, Volume 3, Page(s): 1665 - 1669, 5-9 Sept. 1994.
- [14] S. M. Lee, S. J. Choi, S. T. Yun and Bo H. Cho, "Input Parallel-Output Series Connection of Radial Mode disk-type Piezoelectric Transformer for Thermal Balance Improvement," *PESC2006*, pp.2994-2998, Jun 2006.